



Prof. Lars-Erik Wernersson
Electrical and Information Technology
Lund University

NANOSCIENCE COLLOQUIUM

Thursday
January 26, 2017
at 15:15,
K-space, Fysicum

III-V Nanowire MOSFETs on Si for Millimeter-Wave Applications

III-V Nanowire transistors are candidates to extend the transistor scaling roadmaps. In particular the nMOSFETs have shown a dramatic performance increase the last few years and today their on-state performance is comparable or even superior to other transistor technologies. In particular, the performance strength of the nMOSFETs may be used to enhance the CMOS RF-capabilities what is essential to increase performance and reduce power consumption in millimeter wave systems.

In this talk, we will review efforts made in Lund to realize high-performance III-V nanowire transistors in lateral and vertical geometry. We will present state-of-the-art DC ($g_m > 3 \text{ mS}/\mu\text{m}$) and RF ($f_t/f_{\text{max}} > 300 \text{ GHz}$) performance in both geometries. Nanowire capacitor CV data demonstrating $D_{\text{it}} < 10^{12} \text{ cm}^{-2}$ will be presented and we will discuss the influence of border traps on the transistor frequency response. We will introduce the benefits of source/drain heterostructure design and also present the very first RF-circuits using vertical nanowire MOSFETs. We will also present a III-V vertical nanowire CMOS implementation using InAs and GaSb in a dual channel, single gate stack approach and demonstrate high performance TunnelFEETs using the GaSb/GaAsSb/InAs heterojunction. The latter demonstrating 100x improvement as compared to previous state-of-the-art devices. These results provide key technology for the EU-projects INSIGHT and E²SWITCH.

Host: Heiner Linke (Solid State Physics)

Full program of NanoScience Colloquia
<http://www.nano.lu.se/news-and-events/nanoscience-colloquia>